Notice of Allowability	Application No.	Applicant(s)	
	10/762,459	TAKEUCH ET AL.	
	Examiner	Art Unit	
	Tuan T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 1/23/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *search history printout*.

10/3/05

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 1/23/04 was filed same with the mailing date of the present application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

3. Claims **1-21** are allowed.

4. The following is an examiner's statement of reasons for allowance:

The prior art of record fail to disclose a semiconductor integrated circuit, in combination with other cited limitations, comprising a control circuit which comprises a timeout circuit that controls a cycle operation of the memory cell array, controls operations of the address buffer and the latch circuit, causes the latch circuit latch an address at operation start time, which is output from the address buffer, during the operation of the memory cell array, when the address transition detection circuit detects the transition of the address during the cycle operation, causes the latch circuit to latch, after an end of the operation of the memory cell array, an address that is currently input to the address buffer, and controls to execute the next cycle operation of the memory cell array accordance with the address latched by the latch circuit as recited in claim **1**.

Claims **2-10** are therefore allowed because of their dependency on claim **1**.

The prior art of record fail to disclose a semiconductor integrated circuit, in combination with other cited limitations, comprising an internal CE control circuit which comprises a timeout circuit that controls a cycle operation of the memory cell array, controls a row system circuit and a column system circuit to access the memory cell array and also controls the row address buffer, the column address buffer, the first and second row address latches, and the first and second column address latches on the basis of an AND signal output from the ATD AND circuit, causes the first and second row address latches and the first and second column address latches respectively latch a address and a column address at operation start time, which are output from the row address buffer and the column address buffer, during the operation of the memory cell array, and when the address transition detection circuit detects the transition of the row address or the column address transition detection circuit detects the transition of the column address during the cycle operation, causes the second row address latch and the second column address latch to respectively latch, after an end of the operation the memory cell array, a row address and a column address that are currently latched by the first row address latch and the first column address latch so as to control access to the memory cell array as recited in claim **11**.

Claims **12-19** are therefore allowed because of their dependency on claim **11**.

The prior art of record further fail to disclose an access method for a semiconductor integrated circuit device, in combination with other cited limitations, comprising when the transition the address is detected, to latch, after an end of the causing the latch circuit operation of the memory cell array, an address that currently input to the address buffer; and executing the next cycle operation of the memory cell array in accordance with the address latched by the latch circuit as recited in claim **20**.

The prior art of record further fail to disclose an access method for a semiconductor integrated circuit device, in combination with other cited limitations, comprising when the transition of the row address or column address latch and the second column address latch to respectively latch, after an end of the operation of the memory cell array, a row address and a column address detected, causing the second row address that are currently latched by the first row address latch and the first column address latch; and executing the next cycle operation of the memory cell array in accordance with the addresses latched by the second row address latch and the second column address latch. as recited in claim **21**.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. Coker et al (US 5,528,952) disclose a semiconductor memory with separate timeout control for read and write operations.

b. Sato et al (US 6,882,586) disclose a semiconductor memory device quipped with control circuit for controlling memory cell array in non-normal operation mode.

c. Fukumoto (US 6,370,058) discloses a nonvolatile semiconductor memory device and system LSI including the same.

d. Choi et al. (US 5,625,590) disclose a nonvolatile semiconductor memory device having page buffer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Nguyen whose telephone number is (571) 272-1880. The examiner can normally be reached on Monday - Friday, 7:00 AM - 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Nguyen
Primary Examiner
Art Unit 2824

October 3, 2005